



Features

- Floating high-side driver in bootstrap operation to 600V
- Drives two N-channel MOSFETs or IGBTs in a half bridge configuration
- Outputs tolerant to negative transients
- Programmable dead time to protect MOSFETs
- Wide logic and low side gate driver supply voltage: 10V to 20V
- Wide logic supply voltage offset voltage: -5V to 5V
- Logic input (HIN and LIN*) 3.3V capability
- Schmitt triggered logic inputs with internal pull down
- Undervoltage lockout for high and low side drivers
- Extended temperature range:-40°C to +125°C

Description

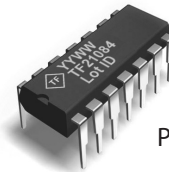
The TF21084 is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half bridge configuration. TF Semiconductor’s high voltage process enables the TF21084’s high side to switch to 600V in a bootstrap operation.

The TF21084 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. Programmable dead time, by an external resistor, provides more system level flexibility.

The TF21084 is offered in PDIP-14 and SOIC-14(N) packages. It operates over an extended -40 °C to +125 °C temperature range.



SOIC-14(N)



PDIP-14

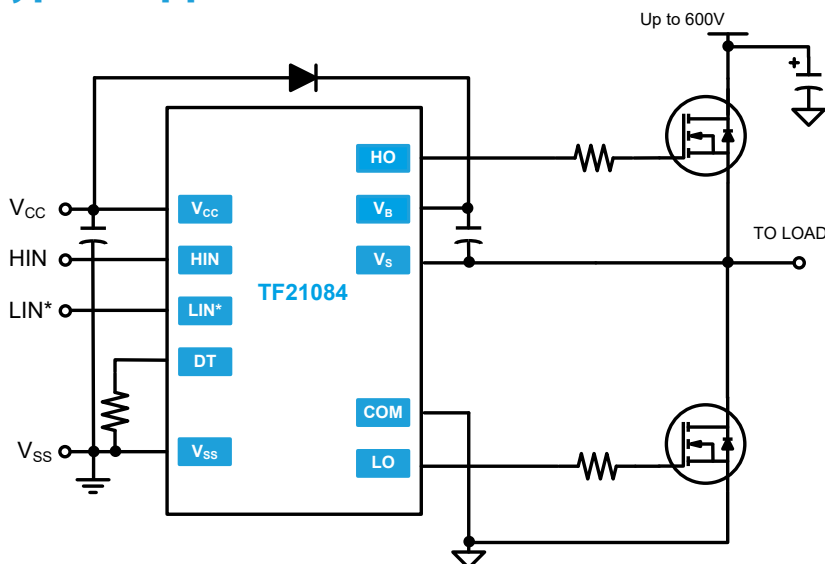
Applications

- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

Ordering Information

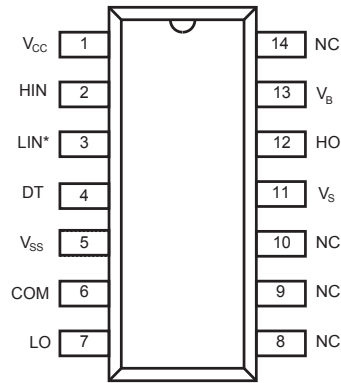
PART NUMBER	PACKAGE	PACK / Qty	Year	Year	Week	Week
			Year	Year	Week	Week
TF21084-TUU	SOIC-14(N)	Tube / 50	YY	WW	TF	TF21084 Lot ID
TF21084-TUH		T&R / 2500				
TF21084-3BS	PDIP-14	Tube / 25	YY	WW	TF	TF21084 Lot ID

Typical Application





Pin Diagrams



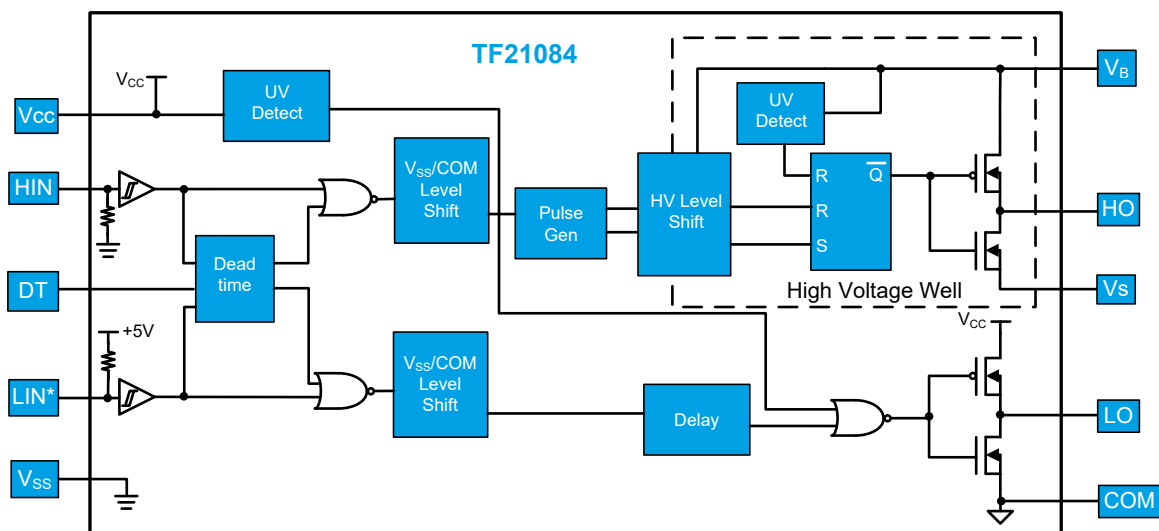
Top View: SOIC-14, PDIP-14

TF21084

Pin Descriptions

PIN NAME	PIN DESCRIPTION
HIN	Logic input for high-side gate driver output, in phase with HO (referenced to VSS).
LIN*	Logic input for low side gate driver output, out of phase with LO (referenced to VSS)
VSS	Logic ground
DT	Programmable deadtime lead, referenced to VSS.
COM	Low-side return
LO	Low-side gate drive output
V _{CC}	Low-side and logic fixed supply
V _B	High-side floating supply
HO	High-side gate drive output
V _S	High-side floating supply return

Functional Block Diagram





Absolute Maximum Ratings (NOTE1)

V_B - High side floating supply voltage.....-0.3V to +624V
 V_S - High side floating supply offset voltage..... V_B -24V to V_B +0.3V
 V_{HO} - High side floating output voltage..... V_S -0.3V to V_B +0.3V
 dV_S/dt - Offset supply voltage transient.....50 V/ns
 V_{DT} - Programmable dead time pin voltage..... V_{SS} -0.3V to V_B +0.3V

V_{CC} - Low side fixed supply voltage.....-0.3V to +24V
 V_{LO} - Low side output voltage.....-0.3V to V_{CC} +0.3V

V_{CC} - Logic supply voltage.....-0.3V to V_{SS} +24V
 V_{SS} - Logic supply offset voltage..... V_{CC} - 25V to V_{CC} +0.3V
 V_{IN} - Logic input voltage (HIN and LIN*)..... V_{SS} - 0.3V to V_{CC} +0.3V

P_D - Package power dissipation at $T_A \leq 25^\circ\text{C}$

SOIC-14.....1.0W
 PDIP-14.....1.6W

NOTE1 Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

SOIC-14 Thermal Resistance (NOTE2)

θ_{JA}120 $^\circ\text{C}/\text{W}$

PDIP-14 Thermal Resistance (NOTE2)

θ_{JA}75 $^\circ\text{C}/\text{W}$

T_J - Junction operating temperature+150 $^\circ\text{C}$

T_L - Lead temperature (soldering, 10s) +300 $^\circ\text{C}$

T_{stg} - Storage temperature range-55 $^\circ\text{C}$ to +150 $^\circ\text{C}$

NOTE2 Thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage	(NOTE 3)	600	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Low side fixed supply voltage	10	20	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{IN}	Logic input voltage (HIN & LIN*)	V_{SS}	5	V
V_{DT}	Programmable deadtime pin voltage	V_{SS}	V_{CC}	V
V_{SS}	Logic ground	-5	5	V
T_A	Ambient temperature	-40	125	$^\circ\text{C}$

NOTE3 Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to - V_{BS} .



DC Electrical Characteristics (NOTE4)

V_{BIAS} (V_{CC} , V_{BS}) = 15V, V_{SS} = COM, and T_A = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage	$V_{CC} = 10V$ to $20V$	2.5			V
V_{IL}	Logic "0" input voltage				0.6	
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	$I_O = 2mA$		0.02	0.2	
V_{OL}	Low level output voltage, V_O	$I_O = 2mA$		0.02	0.1	
I_{LK}	Offset supply leakage current	$V_B = V_S = 600V$			50	μA
I_{BSQ}	Quiescent V_{BS} supply current	$V_{IN} = 0V$ or $5V$	20	75	130	
I_{CCQ}	Quiescent V_{CC} supply current	$V_{IN} = 0V$ or $5V$, $RDT = 0 \Omega$	0.4	1.0	1.6	mA
I_{IN+}	Logic "1" input bias current	$HIN = 5V$, $LIN^* = 0V$		5	20	μA
I_{IN-}	Logic "0" input bias current	$HIN = 0V$, $LIN^* = 5V$			5	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		8.0	8.9	9.8	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold		7.4	8.2	9.0	
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		8.0	8.9	9.8	
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		7.4	8.2	9.0	
V_{CCUV+}	Hysteresis		0.3	0.7		V
V_{BSUV+}						
I_{O+}	Output high short circuit pulsed current	$V_O = 0V$, $PW \leq 10 \mu s$	120	290		mA
I_{O-}	Output low short circuit pulsed current	$V_O = 15V$, $PW \leq 10 \mu s$	250	600		

NOTE4 The V_{IN} , V_{th} , I_{IN} parameters are referenced to V_{SS} and are applicable to the two logic input pins: HIN and LIN^* . The V_O and I_O parameters are referenced to COM and are applicable to the respective output pins: HO and LO .

AC Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V$, $V_{SS} = COM$, $C_L = 1000$ pF, and $T_A = 25$ °C unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{ON}	Turn-on propagation delay	$V_S = 0V$		220	300	ns
t_{OFF}	Turn-off propagation delay	$V_S = 0V$ or 600V		200	280	
$t_{DM ON}$	Delay matchng $ t_{ON} - t_{OFF} $			0	30	
t_r	Turn-on rise time	$V_S = 0V$		100	220	
t_f	Turn-off fall time			35	80	
t_{DT}	Deadtime: $t_{DT LO-HO}$ & $t_{DT HO-LO}$	$R_{DT} = 0\Omega$	400	540	680	μs
		$R_{DT} = 200k\Omega$, NOTE5	4	5	6	
t_{MDT}	Deadtime matching = $t_{DT LO-HO} - t_{DT HO-LO}$	$R_{DT} = 0\Omega$		0	60	ns
		$R_{DT} = 200k\Omega$		0	600	

NOTE5 Guaranteed by design, not tested in production

Timing Waveforms

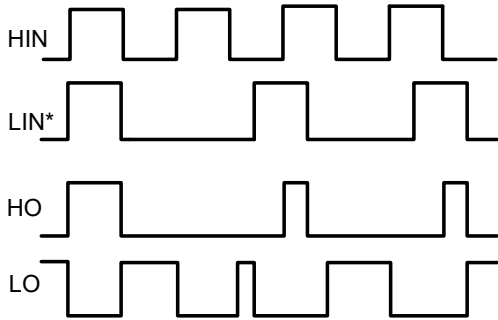


Figure 1. Input / Output Timing Diagram

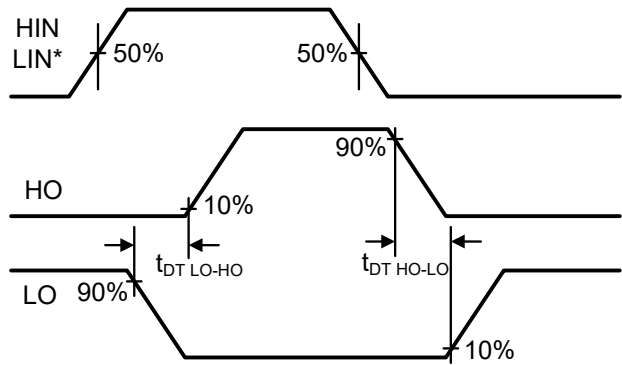


Figure 2. Deadtime Waveform Definitions

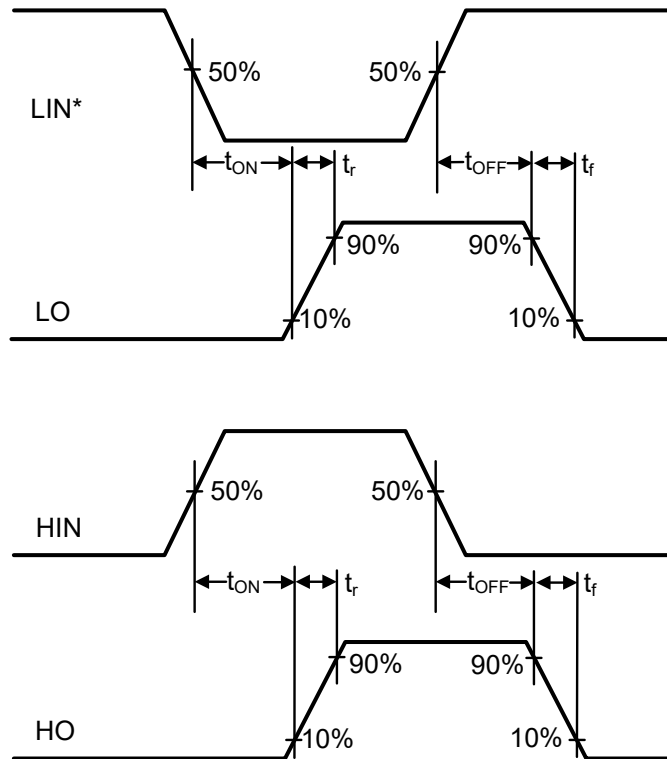


Figure 3. Switching Time Waveform Definitions

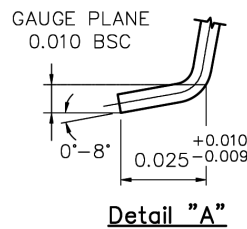
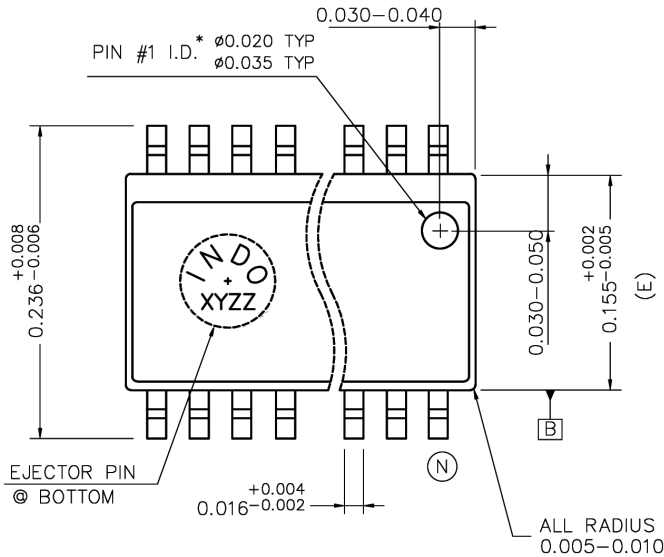
Package Dimensions (SOIC-14N)

Please contact support@tfsemi.com for package availability.

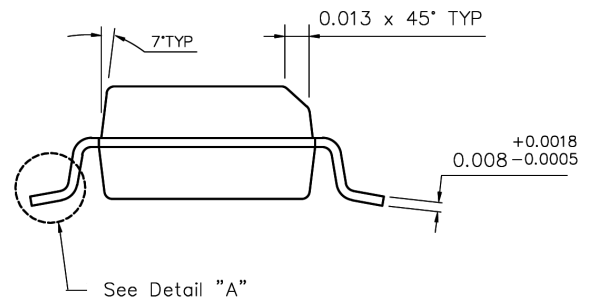
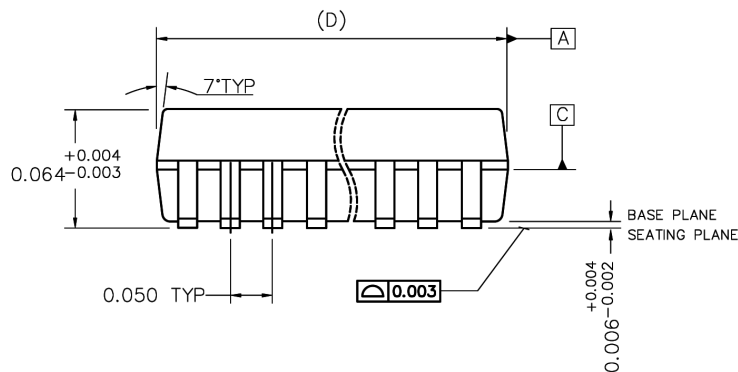
ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE NOTED

NOTES:

1. "D" & "E" ARE REFERENCE DATUMS AND DO NOT INCLUDE MOLD FLASH OR PROTRUSION. MOLD FLASH OR PROTRUSION SHALL NOT EXCEED 6 MILS PER SIDE.
2. "N" IS THE NUMBER OF TERMINAL POSITIONS.
3. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 3 MILS! (● SEATING PLANE) OUTGOING ASSEMBLY & 4 MILS AFTER TEST.
4. THE BOTTOM PACKAGE LEAD SIDE MAY BE BIGGER THAN THE TOP PACKAGE LEAD SIDE BY 4 MILS (2 MILS PER SIDE). BOTTOM PACKAGE DIMENSION SHALL FOLLOW DIMENSION STATED IN THIS DRAWING.
5. THE BOTTOM EJECTOR PIN CONTAINS COUNTRY OF ORIGIN "INDO" AND MOLD ID. (REFER TO TABLE FOR OPTION).
6. THIS DRAWING CONFORMS TO JEDEC REF. MS-012 REV. E



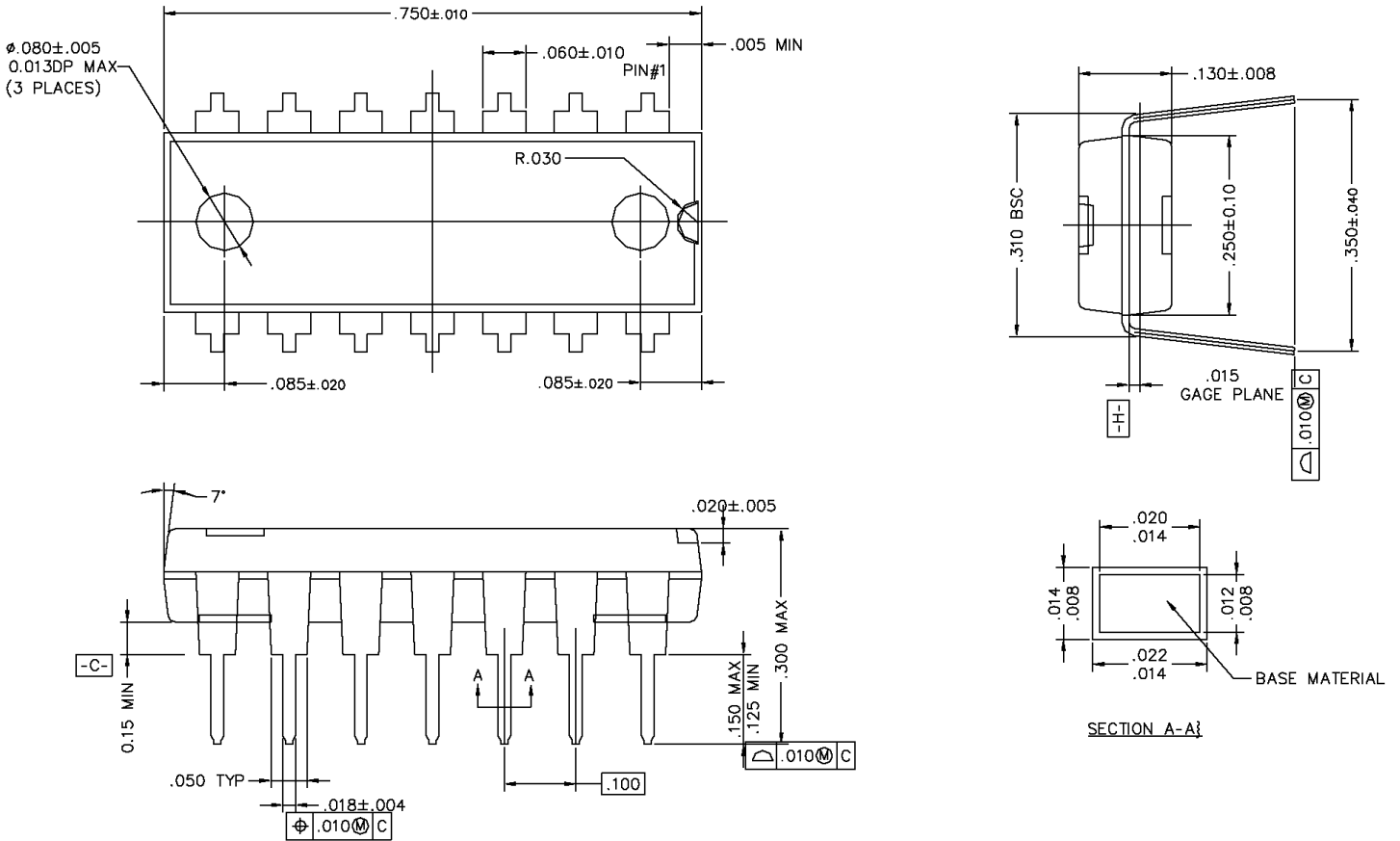
N	D VARIATION			MGP MOLD			
	MIN	NOM	MAX	PIN 1 I.D.	EJECT PIN	PIN 1 I.D.	EJECT PIN
08	0.189	0.193	0.196	N/A	YES	YES	YES
14	0.337	0.339	0.344	YES	NO	YES	YES
16	0.386	0.390	0.393	N/A	YES	YES	YES



Package Dimensions (PDIP-14)

Please contact support@tfsemi.com for package availability.

ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE NOTED



Note: Drawing conforms to jedec ref. MS-001 rev D

Revision History

Rev.	Change	Owner	Date
1.0	First release, AI datasheet	Keith Spaulding	7/6/2015
1.1	Text edit	Keith Spaulding	7/18/2017

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