



TF1636

3-Phase Half-Bridge Gate Driver

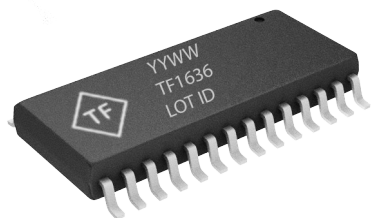
Features

- Three floating high-side drivers in bootstrap operation to 250V
- 200mA source / 350mA sink output current capability
- Outputs tolerant to negative transients, dV/dt immune
- Logic input 3.3V capability
- Internal deadtime of 290ns to protect MOSFETs
- Matched prop delay for all channels
- Outputs out of phase with inputs
- Schmitt triggered logic inputs
- Cross conduction prevention logic
- Undervoltage lockout for all channels
- Overcurrent protection shuts down drivers
- Extended temperature range: -40°C to +125°C

Applications

- 3-Phase Motor Inverter Driver
- BLDC Motor Driver
- Industrial Motor Inverter - Power Tools, Robotics
- General Purpose 3-Phase Inverter

SOIC-28



Description

The TF1636 is a three-phase gate driver IC designed for high voltage, high speed applications, driving N-channel MOSFETs and IGBTs in a half-bridge configuration. TF Semiconductor's high voltage process enables the TF1636 high sides to switch to 250V in a bootstrap operation.

The TF1636 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices and are enabled low to better function in high noise environments. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction.

The TF1636 offers numerous protection functions. A shoot-through protection logic prevents both outputs being high with both inputs high (fault state), an undervoltage lockout for V_{CC} shuts down all drivers through an internal fault control, and a UVLO for V_{BS} shuts down the respective high side output. Also an overcurrent protection will terminate the six outputs. Both the V_{CC} UVLO and the overcurrent protection trip an automatic fault clear with a timing that is adjustable with an external capacitor.

The TF1636 is offered in SOIC 28 package and operates over an extended -40 °C to +125 °C temperature range.

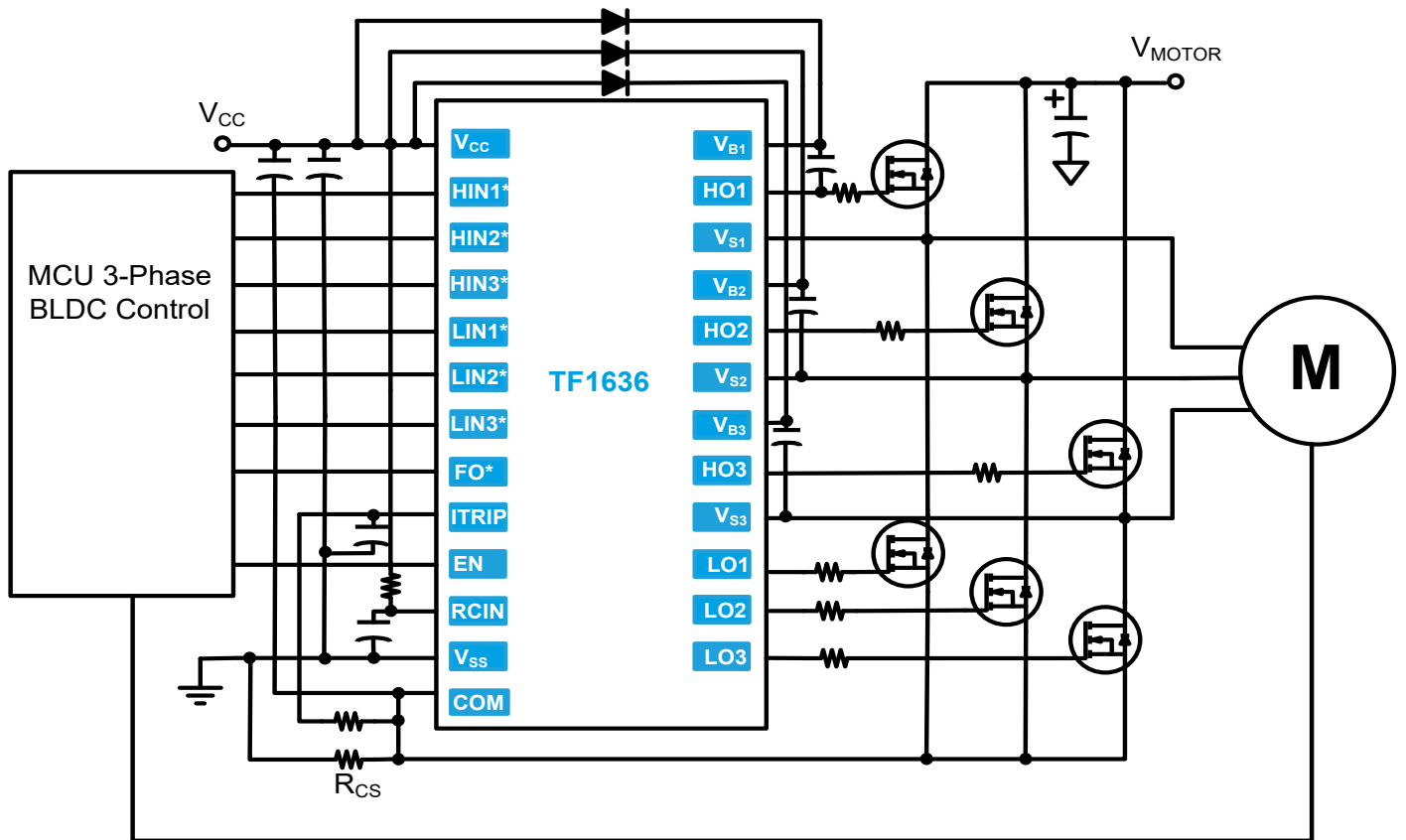
Ordering Information

Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF1636-TLS	SOIC-28	Tube / 25	YYWW TF1636
TF1636-TLH	SOIC-28	T&R / 1500	Lot ID

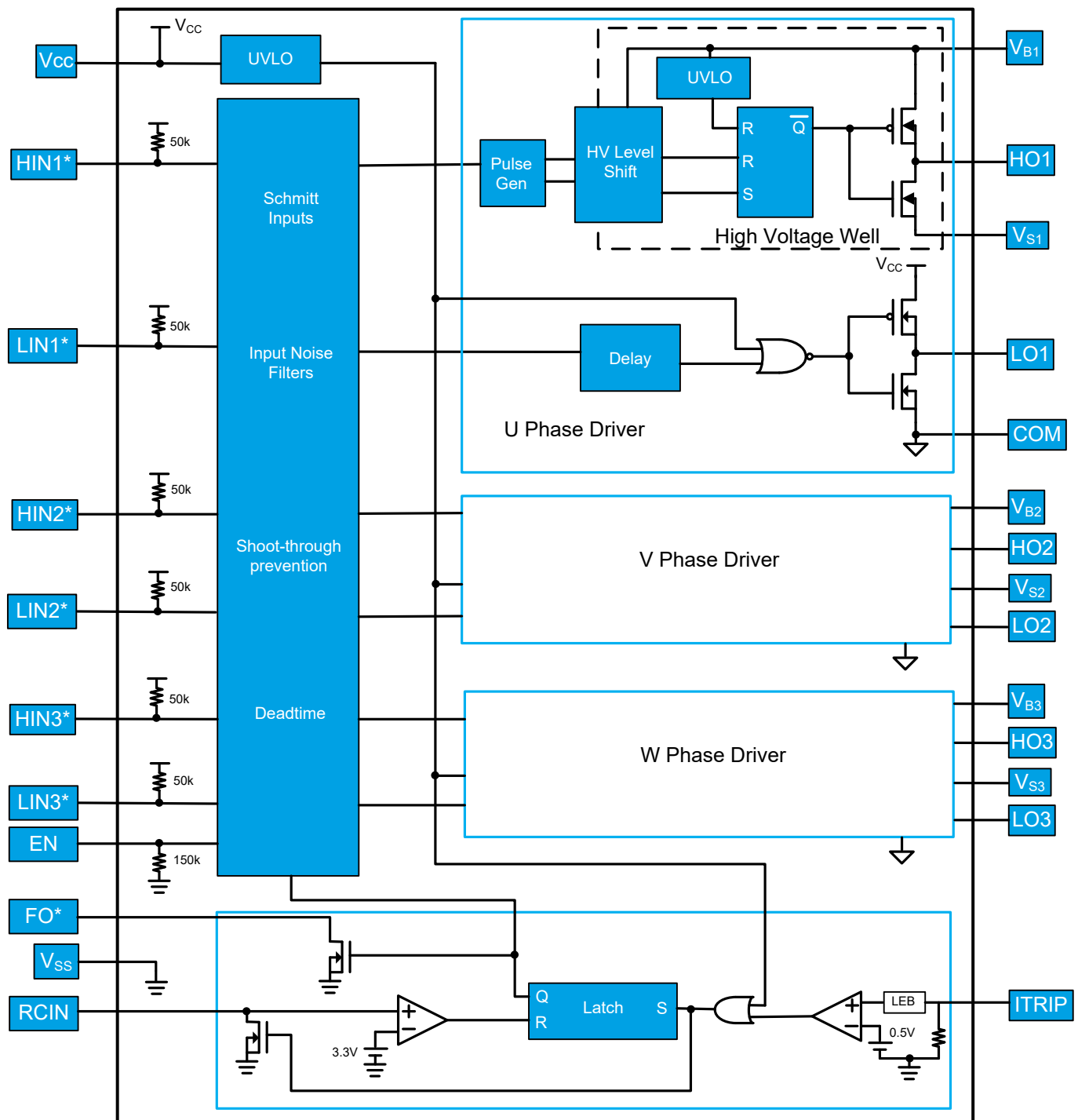


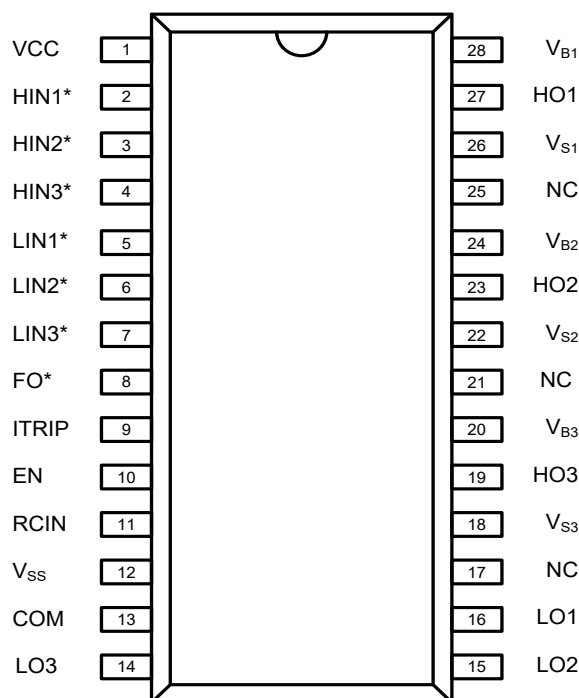
Typical Application





Functional Block Diagram





Top View: SOIC-28

Pin Descriptions

PIN NAME	PIN NUMBER	PIN DESCRIPTION
VCC	1	Low-side and logic fixed supply
HIN1*, HIN2*, HIN3*	2, 3, 4	Logic input for high-side gate driver output, out of phase with HO.
LIN1*, LIN2*, LIN3*	5, 6, 7	Logic input for low-side gate driver output, out of phase with LO.
FO*	8	Fault output with open drain (fault with over-current and VCC UVLO)
ITRIP	9	Analog input for over-current shutdown
EN	10	Logic input for functionality, I/O logic functions when EN is high.
RCIN	11	An external RC network input used to define FAULT CLEAR delay
V _{SS}	12	Logic ground
COM	13	Low-side driver return
LO3, LO2, LO1	14, 15, 16	Low-side gate driver output
NC	17, 21, 25	No Connect
V _{S3} , V _{S2} , V _{S1}	18, 22, 26	High-side floating supply return
HO3, HO2, HO1	19, 23, 27	High-side gate driver output
V _{B3} , V _{B2} , V _{B1}	20, 24, 28	High-side floating supply



Absolute Maximum Ratings (NOTE1)

V_B - High-side floating supply voltage.....-0.3V to +274V
 V_S - High-side floating supply offset voltage... V_B -24V to V_B +0.3V
 V_{HO} - High-side floating output voltage..... V_S -0.3V to V_B +0.3V
 V_{LO} - Low-side output voltage.....-0.3V to V_{CC} +0.3V
 dV_S/dt - Offset supply voltage transient.....50V/ns
 V_{CC} - Low-side fixed supply voltage.....-0.3V to +24V
 V_{IN} - Logic input voltage (HIN*, LIN*, ITRIP, and EN).....-0.3V to 5.5V

NOTE1 Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

P_D - Package power dissipation at $T_A \leq 25^\circ\text{C}$
 SOIC-28.....2.3W

SOIC-28 Thermal Resistance (NOTE2)

θ_{JC}45 $^\circ\text{C}/\text{W}$
 θ_{JA}60 $^\circ\text{C}/\text{W}$

T_J - Junction operating temperature.....+150 $^\circ\text{C}$
 T_L - Lead Temperature (soldering, 10 seconds).....+300 $^\circ\text{C}$
 T_{stg} - Storage temperature-55 to 150 $^\circ\text{C}$

NOTE2 Thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage	NOTE3	250	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Low side fixed supply voltage	10	20	V
V_{LO}	Low side output voltage	COM	V_{CC}	V
V_{IN}	Logic input voltage (HIN*, LIN*, ITRIP, and EN)	V_{SS}	5	V
V_{FO}	Fault output Voltage	V_{SS}	V_{CC}	V
V_{SS}	Logic Ground	-5	5	C
T_A	Ambient temperature	-40	125	$^\circ\text{C}$

NOTE3 Logic operational for VS of -5V to +250V. Logic state held for VS of -5V to -VBS



DC Electrical Characteristics (NOTE4)

$V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25^\circ C$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "0" input voltage		2.5			V
V_{IL}	Logic "1" input voltage					
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	$I_O = 0mA$			0.1	V
V_{OL}	Low level output voltage, V_O	$I_O = 0mA$			0.1	
I_{LK}	Offset supply leakage current	$V_B = V_S = 250V$			10	μA
I_{BSQ}	Quiescent V_{BS} supply current	$V_{IN} = 0V$ or $5V, EN=0V$	10	50	80	
I_{CCQ}	Quiescent V_{CC} supply current	$V_{IN} = 0V$ or $5V, EN=0V$		200		μA
I_{IN+}	Logic input bias current (HO=LO=HIGH)	$V_{IN} = 0V$		100		μA
I_{IN-}	Logic input bias current (HO=LO=LOW)	$V_{IN} = 5V$		8.5	25	
I_{EN+}	Logic Enable "1" input bias current	$V_{EN} = 5V$		33		μA
I_{EN-}	Logic Enable "0" input bias current	$V_{EN} = 0V$			2	μA
V_{BSUV+} V_{CCUV+}	V_{BS} and V_{CC} supply under-voltage positive going threshold		7.5	8.5	9.3	V
V_{BSUV-} V_{CCUV-}	V_{BS} and V_{CC} supply under-voltage negative going threshold		7.0	8.0	8.7	
I_{O+}	Output high short circuit pulsed current	$V_O = 0V, PW \leq 10 \mu s$	120	200		mA
I_{O-}	Output low short circuit pulsed current	$V_O = 15V, PW \leq 10 \mu s$	250	350		
V_{ITH+}	Overcurrent detect positive threshold		400	500	600	mV
V_{ITH-}	Overcurrent detect negative threshold			440		mV
I_{CSIN}	Short-circuit input current	$V_{ITRIPIN}=1V$	5	10	15	μA
I_{SOFT}	Soft turn-off sink current		25	40	55	μA
V_{RCINT+}	RCIN Positive going threshold voltage			8		V
V_{RCINT-}	RCIN Nositive going threshold voltage			5		V
V_{FOL}	Fault output low level voltage	$V_{CS}=1V, I_{FO}=1.5mA$		0.2	0.5	V
R_{DSRCIN}	RCIN On resistance	$I_{RCIN}=1.5mA$	50	75	100	Ω
R_{DSFO}	Fault output on resistance	$I_{FO}=1.5mA$	90	130	170	Ω

NOTE4 The V_{IN} , V_{TH} , and I_{IN} parameters are referenced to V_{SS} and are applicable to all six channels (HIN1,2,3* and LIN1,2,3*). The V_O and I_O parameters are applicable to the outputs (HO1,2,3* and LO1,2,3* and are referenced to COM.



AC Electrical Characteristics

$V_{BIAS} (V_{CC}, V_{BS}) = 15V$, $C_L = 1000pF$, $C_{RCIN} = 2nF$, and $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{on}	Turn-on propagation delay	$V_S = 0V$	350	500	650	ns
t_{off}	Turn-off propagation delay	$V_S = 0V$	350	500	650	
t_r	Turn-on rise time	$V_S = 0V$		125	190	
t_f	Turn-off fall time			50	75	
t_{DM}	Delay matching				50	ns
t_{EN}	Enable low to output shutdown delay		400	500	600	ns
t_{BLT}	ITRIP Pin leading-edge blanking time		200	300	400	ns
t_{FLT}	Time from ITRIP triggering to FO*	From $V_{ITRIP} = 1V$ to FO* turn off		630		ns
t_{ITRIP}	Time from ITRIP triggering to all gate outputs turn off	From $V_{ITRIP} = 1V$ to starting gate turn off		640		ns
t_{FLTIN}	Input filtering time (HIN*, LIN*, EN)		200	250	300	ns
t_{FLTCLR}	Fault clear time			1.3		ms
t_{DT}	Deadtime		230	290	350	ns
t_{DTM}	Deadtime matching				50	ns
t_{PM}	Output pulse width matching (NOTES)	$PW_{IN} > 1\mu s$		50	100	ns

NOTES t_{PM} is defined as $PW_{IN} - PW_{OUT}$.



Timing Waveforms

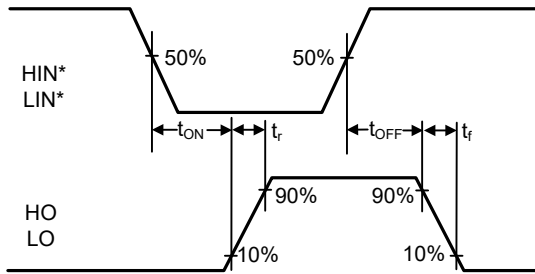


Figure 1. Switching Time Waveform Definitions

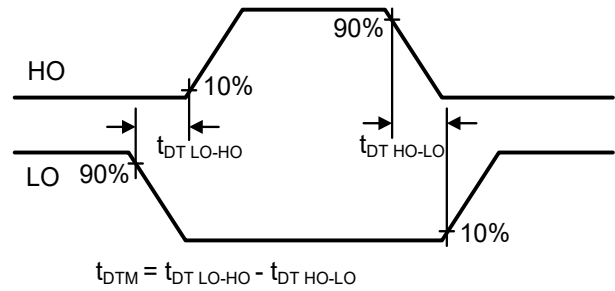


Figure 2. Deadtime Waveform Definitions

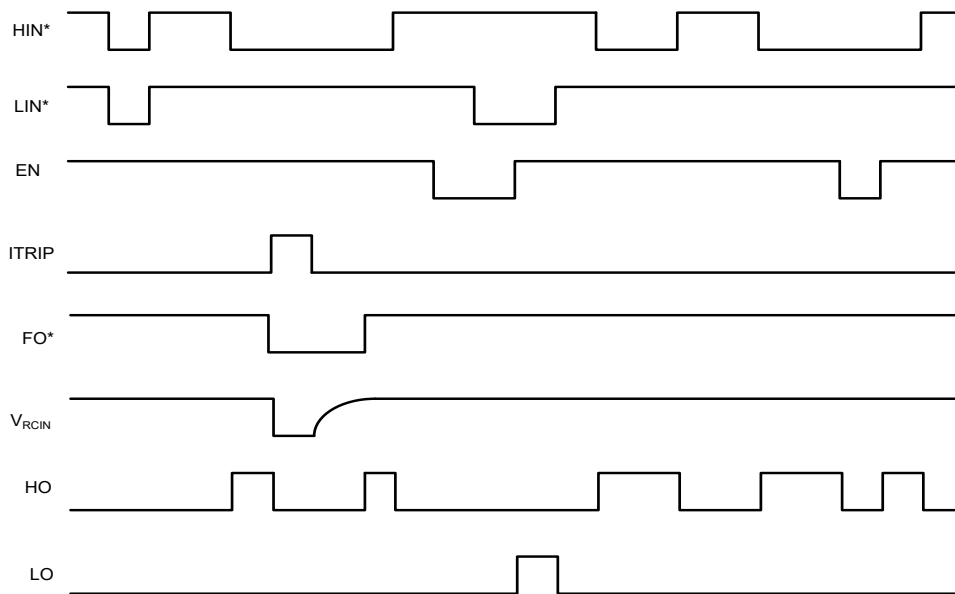


Figure 3. Input/Output Timing Diagram

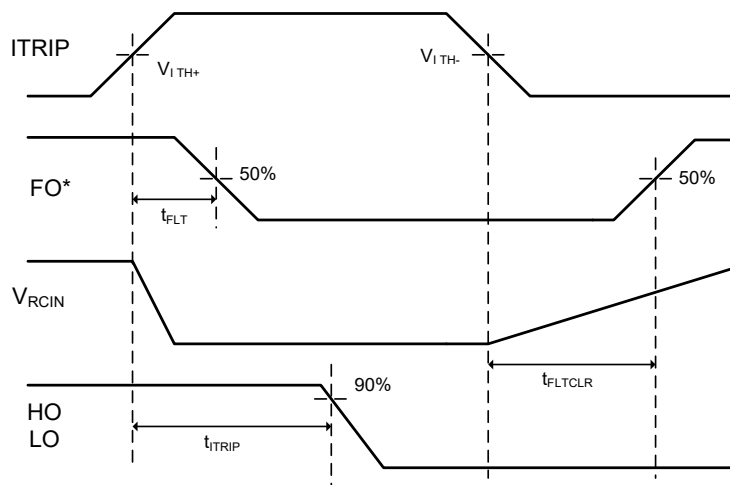
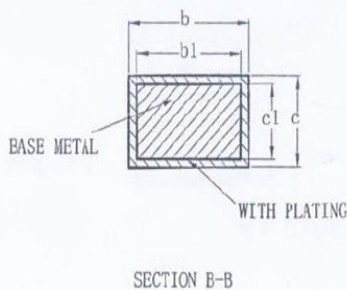
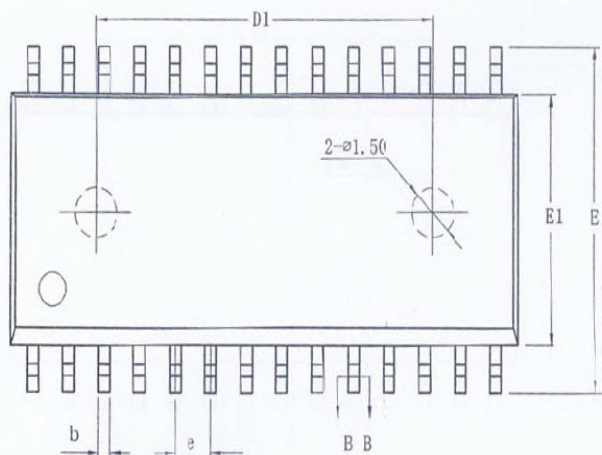
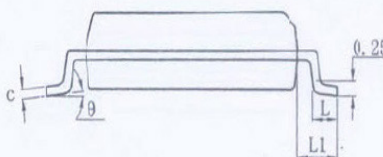
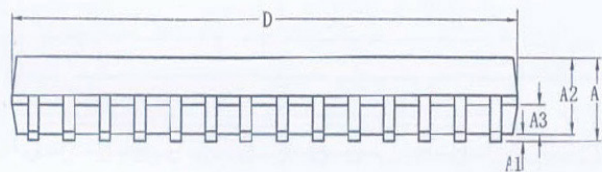


Figure 4. Overcurrent Timing Definitions



Package Dimensions (SOIC-28)

Please contact support@tfsemi.com for package availability.



SYMBL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	2.65
A1	0.10	—	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.39	—	0.48
b1	0.38	0.41	0.43
c	0.25	—	0.31
c1	0.24	0.25	0.26
D	17.80	18.00	18.20
D1	11.90	12.00	12.10
E	10.10	10.30	10.50
E1	7.30	7.50	7.70
e	1.27BSC		
L	0.70	—	1.00
L1	1.40BSC		
•	0	—	8°
	120°120		



Revision History

Rev.	Change	Owner	Date
1.0	First release AI datasheet	Keith Spaulding	5/20/2015
2.0	Revision system added	Keith Spaulding	1/20/2016
2.1	Deadtime waveform definition, fig. 2 added	Keith Spaulding	3/22/2016
2.2	Edit text	Keith Spaulding	1/25/2018

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