



TF0507A

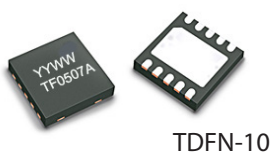
High Frequency Half-Bridge Gate Driver

Features

- Drives two N-channel MOSFETs in a half bridge configuration
- Floating high-side driver in bootstrap operation to 50V
- 1.5A source / 2.0A sink output current capability
- Internal bootstrap diode included
- Undervoltage lockout for high and low side drivers
- Delay matching a maximum of 5ns
- Propagation delay a typical of 20ns
- Ultra low standby current (<1μA)
- Logic input (HIN, LIN, and EN) 3.3V capability
- Extended temperature range: -40°C to +125°C
- Space saving TDFN-10 3x3mm package

Applications

- BLDC Motor Drivers
- Battery Powered Hand Tools
- DC/DC converters
- eCig devices



TDFN-10

Description

The TF0507A is a high frequency gate driver capable of driving N-channel MOSFETs in a half bridge configuration. The floating high-side driver can switch to 50V in a bootstrap configuration.

The TF0507A logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with MCUs. UVLO for high side and low side will protect MOSFET with loss of supply. Also to protect MOSFETs, cross conduction prevention logic prevents the HO and LO to be on at the same time.

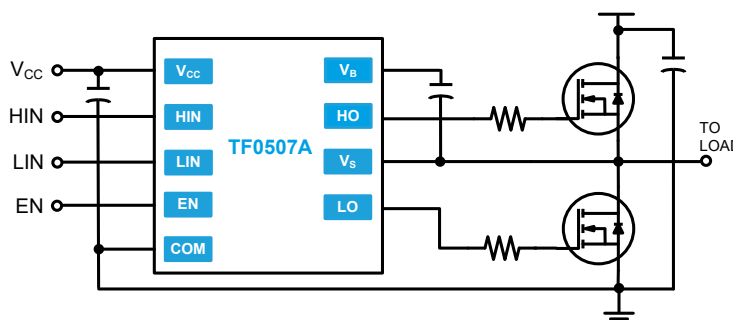
Fast and well matched propagation delays allow a higher switching frequency, enabling a smaller, more compact power switching design using smaller associated components. Also to minimize space an internal bootstrap diode is included and the TF0507A comes in a space-saving TDFN-10 package. It operates over an extended -40 °C to +125 °C temperature range.

Ordering Information

Year Year Week Week

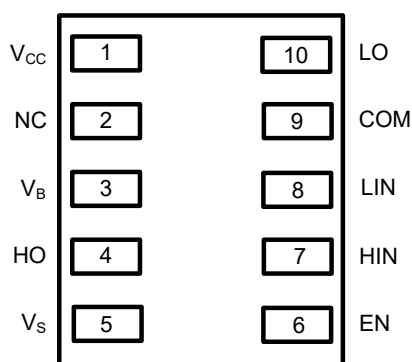
PART NUMBER	PACKAGE	PACK / Qty	MARK
TF0507A-NHS	TDFN-10	Tube / 120	YYWW TF0507A
TF0507A-NHP	TDFN-10	T&R / 3,000	

Typical Application





Pin Diagrams

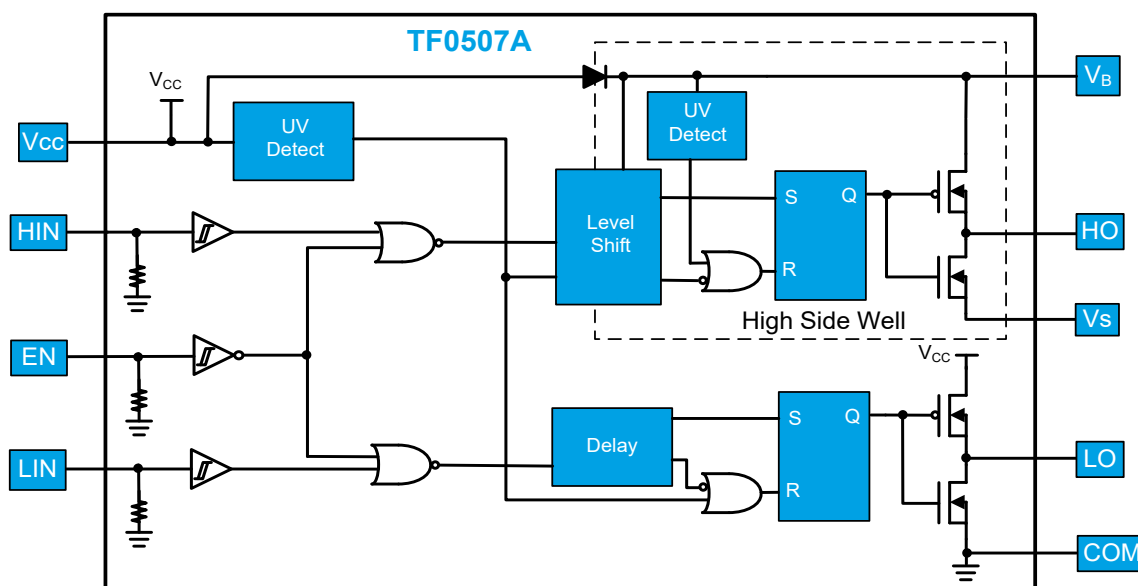


Top View: TDFN-10

Pin Descriptions

PIN NAME	PIN NUMBER	PIN DESCRIPTION
V _{CC}	1	Low-side and logic fixed supply
NC	2	No Connect
V _B	3	High-side floating supply
HO	4	High-side gate driver output
V _S	5	High-side floating supply return
EN	6	Logic input enable, a logic low turns off gate drivers
HIN	7	Logic input for high-side gate driver, in phase with HO
LIN	8	Logic input for low-side gate driver, in phase with LO
COM	9	Low-side and logic return
LO	10	Low-side gate drive output
COM	PAD	Low-side and logic return

Functional Block Diagram





Absolute Maximum Ratings (NOTE1)

V_B - High side floating positive supply voltage.....0.3V to 60V
 V_S - High side floating negative supply voltage.. V_B -14V to V_B +0.3V
 V_{HO} - Highside floating output voltage..... V_S -0.3V to V_B +0.3V
 dV_S/dt - Offset supply voltage transient.....50V/ns

V_{CC} - Logic and Low-side fixed supply voltage.....-0.3V to +14V
 V_{LO} - Low-side output voltage.....-0.3V to V_{CC} +0.3V
 V_{IN} - Logic input voltage (HIN, LIN, and EN).....-0.3V to V_{CC} +0.3V

NOTE1 Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

P_D - Package power dissipation at $T_A \leq 25^\circ\text{C}$
 TDFN-10.....0.4W

TDFN-10 Thermal Resistance (NOTE2)

θ_{JA}64°C/W
 θ_{JC}42°C/W

T_J - Junction operating temperature.....-40°C to +150°C
 T_L - Lead Temperature (soldering, 10 seconds).....+300°C
 T_{stg} - Storage temperature-55°C to 150°C

NOTE2 When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply	$V_S + 8$	$V_S + 14$	V
V_S	High side floating supply offset voltage	NOTE3	50	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Logic and Low side fixed supply voltage	8	14	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{IN}	Logic input voltage (HIN, LIN and EN)	0	5	V
T_A	Ambient temperature	-40	125	°C

NOTE3 Logic operational for V_S of -5V to +50V.



DC Electrical Characteristics (NOTE4)

$V_{CC} = V_{BS} = 12V$, $COM = V_S = 0V$, $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" input voltage		2.4			V
V_{IL}	Logic "0" input voltage				0.8	
V_{ENIH}	Enable logic "1" input voltage		1.5			
V_{ENIL}	Enable logic "0" input voltage				0.7	
V_{INHYS}	Input voltage hysteresis			0.6		
$V_{ENINHYS}$	Enable input voltage hysteresis			0.1		
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	$I_{O+} = 100\text{mA}$		0.45	0.6	
V_{OL}	Low level output voltage, V_O	$I_{O-} = 100\text{mA}$		0.15	0.22	
I_{LK}	Offset supply leakage current	$V_B = V_S = 60V$		1	5	μA
I_{CCSD}	V_{CC} shutdown supply current	$V_{IN} = 0V$ or $5V$, $V_{EN} = 0V$		0	1	
I_{CCQ}	V_{CC} quiescent supply current	$V_{IN} = 0V$ or $5V$		130	200	
I_{CCOP}	V_{CC} operating supply current	$f_s = 500\text{kHz}$, $C_L = 1000\text{pF}$		7.3		mA
I_{BSQ}	V_{BS} quiescent supply current	$V_{IN} = 0V$ or $5V$		40	100	μA
I_{BSOP}	V_{BS} operating supply current	$f_s = 500\text{kHz}$, $C_L = 1000\text{pF}$		7.3		mA
I_{IN+}	Logic "1" input bias current	$V_{IN} = 5V$			50	μA
I_{IN-}	Logic "0" input bias current	$V_{IN} = 0V$			5	
I_{ENIN+}	Enable logic "1" input bias current	$V_{IN} = 5V$		43	60	
I_{ENIN-}	Enable logic "0" input bias current	$V_{IN} = 0V$		0	5	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		6.0	7.0	8.0	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold		5.6	6.6	7.6	
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		6.0	7.0	8.0	
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		5.6	6.6	7.6	
I_{O+}	Output high short circuit pulsed current	$V_O = 0V$, $PW \leq 10\text{ }\mu\text{s}$	0.9	1.5		A
I_{O-}	Output low short circuit pulsed current	$V_O = 15V$, $PW \leq 10\text{ }\mu\text{s}$	1.5	2.0		
V_{F1}	Forward voltage of bootstrap diode	$I_F = 100\mu\text{A}$		0.67		V
V_{F2}	Forward voltage of bootstrap diode	$I_F = 100\text{mA}$		1.7		V

NOTE4 The V_{IN} and I_{IN} parameters are applicable to the logic input pins: HIN, LIN, and EN. The V_O and I_O parameters are applicable to the respective output pins: HO and LO



AC Electrical Characteristics

$V_{CC} = V_{BS} = 12V$, $COM = V_S = 0V$, $C_L = 1000pF$, $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{on}	Turn-on propagation delay			20	35	ns
t_{off}	Turn-off propagation delay	$V_S = 50V$		23	56	
t_{DM}	Delay matching, HS & LS turn-on				5	
t_r	Turn-on rise time			16	30	
t_f	Turn-off fall time			12	25	



Timing Waveforms

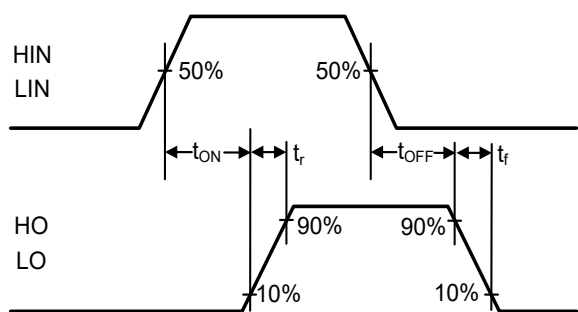


Figure 1. Switching Time Waveform Definitions

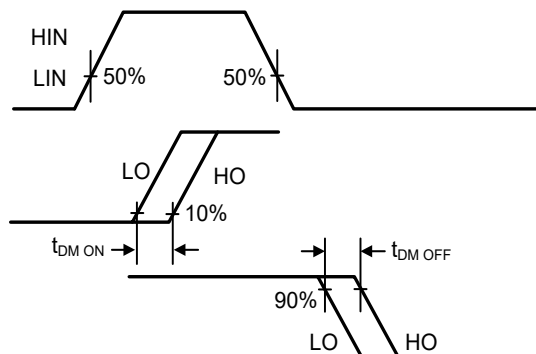


Figure 2. Delay Matching Waveform Definitions

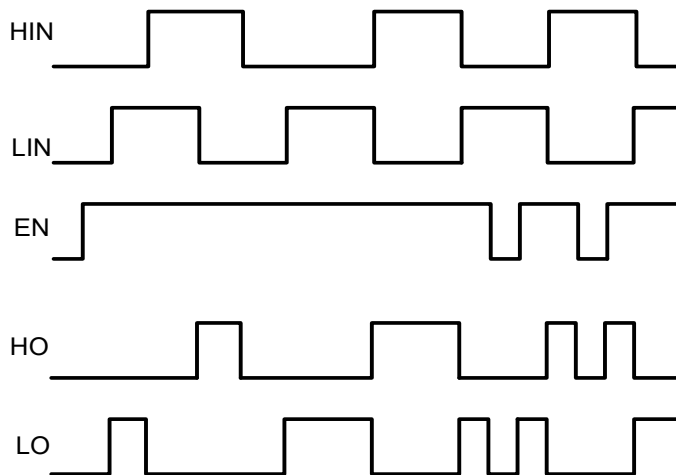
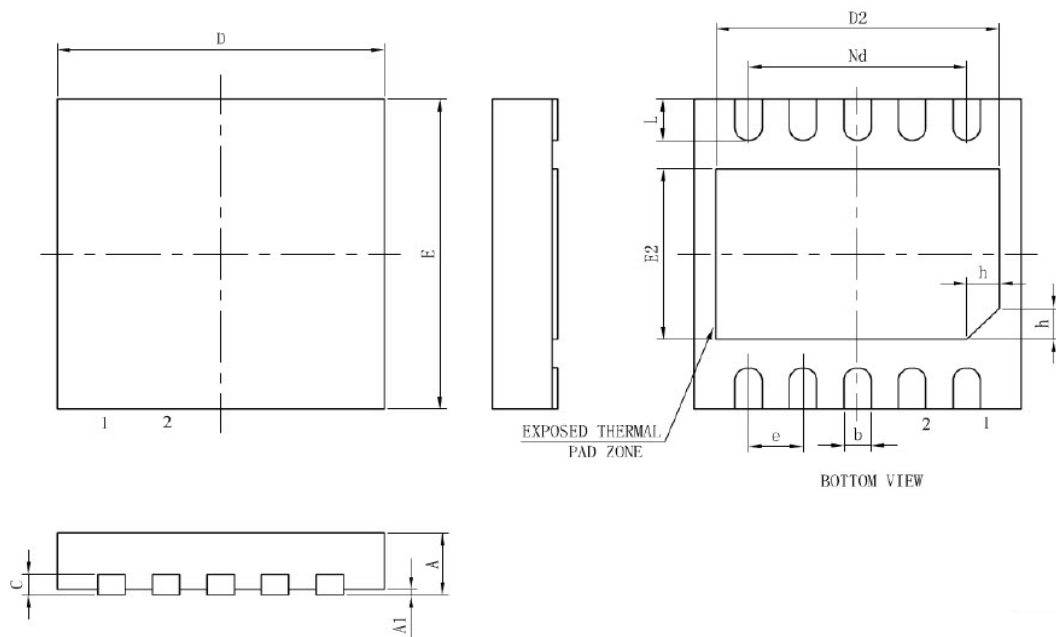


Figure 3. Input / Output Timing Diagram



Package Dimensions (TDFN-10)

Please contact support@tfsemi.com for package availability.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
c	0.50BSC		
Nd	2.00BSC		
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
L	0.30	0.40	0.50
h	0.20	0.25	0.30



Revision History

Rev.	Change	Owner	Date
1.0	First release	Keith Spaulding	10/3/17

Important Notice

TF Semiconductor Solutions (TFSS) PRODUCTS ARE NEITHER DESIGNED NOR INTENDED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS UNLESS THE SPECIFIC TFSS PRODUCTS ARE SPECIFICALLY DESIGNATED BY TFSS FOR SUCH USE. BUYERS ACKNOWLEDGE AND AGREE THAT ANY SUCH USE OF TFSS PRODUCTS WHICH TFSS HAS NOT DESIGNATED FOR USE IN MILITARY AND/OR AEROSPACE, AUTOMOTIVE OR MEDICAL DEVICES OR SYSTEMS IS SOLELY AT THE BUYER'S RISK.

TFSS assumes no liability for application assistance or customer product design. Customers are responsible for their products and applications using TFSS products.

Resale of TFSS products or services with statements different from or beyond the parameters stated by TFSS for that product or service voids all express and any implied warranties for the associated TFSS product or service. TFSS is not responsible or liable for any such statements.

©2017 TFSS. All Rights Reserved. Information and data in this document are owned by TFSS wholly and may not be edited, reproduced, or redistributed in any way without the express written consent from TFSS.

For additional information please contact support@tfsemi.com or visit www.tfsemi.com.