



TF0504

Half-Bridge Gate Driver

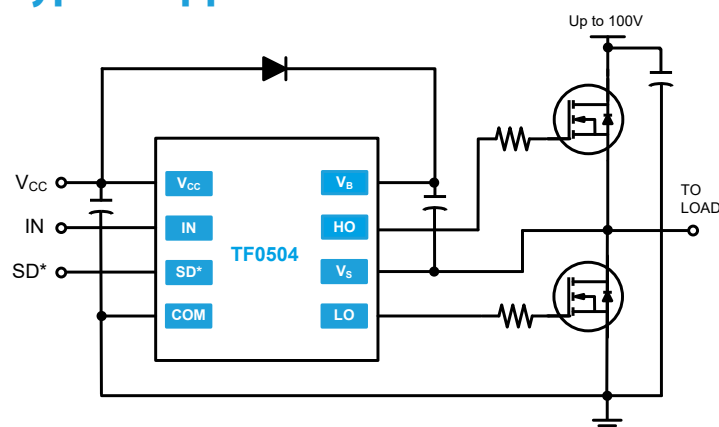
Features

- Floating high-side driver in bootstrap operation to 100V
- Drives two N-channel MOSFETs or IGBTs in a half bridge configuration
- 290mA source/600mA sink output current capability
- Outputs tolerant to negative transients
- Internal dead time of 430ns to protect MOSFETs
- Wide low side gate driver supply voltage: 10V to 20V
- Logic input (IN and SD*) 3.3V capability
- Schmitt triggered logic inputs
- Undervoltage lockout for V_{CC} (logic and low side supply)
- Extended temperature range: -40°C to +125°C

Applications

- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

Typical Application



Description

The TF0504 is a high voltage, high speed gate driver capable of driving N-channel MOSFETs and IGBTs in a half bridge configuration. TF Semiconductor's high voltage process enables the TF0504's high side to switch to 100V in a bootstrap operation.

The TF0504 logic inputs are compatible with standard TTL and CMOS levels (down to 3.3V) to interface easily with controlling devices. The driver outputs feature high pulse current buffers designed for minimum driver cross conduction. TF0504 has a fixed internal deadtime of 430ns (typical).

The TF0504 is offered in a TDFN-10 and operates over an extended -40 °C to +125 °C temperature range.

TDFN-10



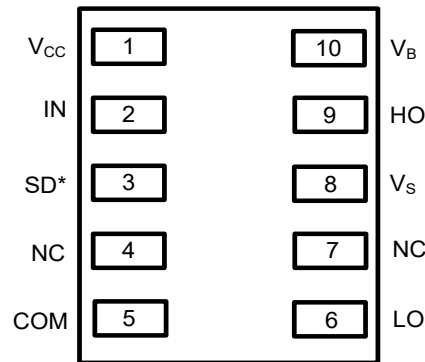
Ordering Information

Year Year Week Week

PART NUMBER	PACKAGE	PACK / Qty	MARK
TF0504-NHS	TDFN-10	Tube / 120	YYWW
TF0504-NHP	TDFN-10	T&R / 3,000	TF0504



Pin Diagrams



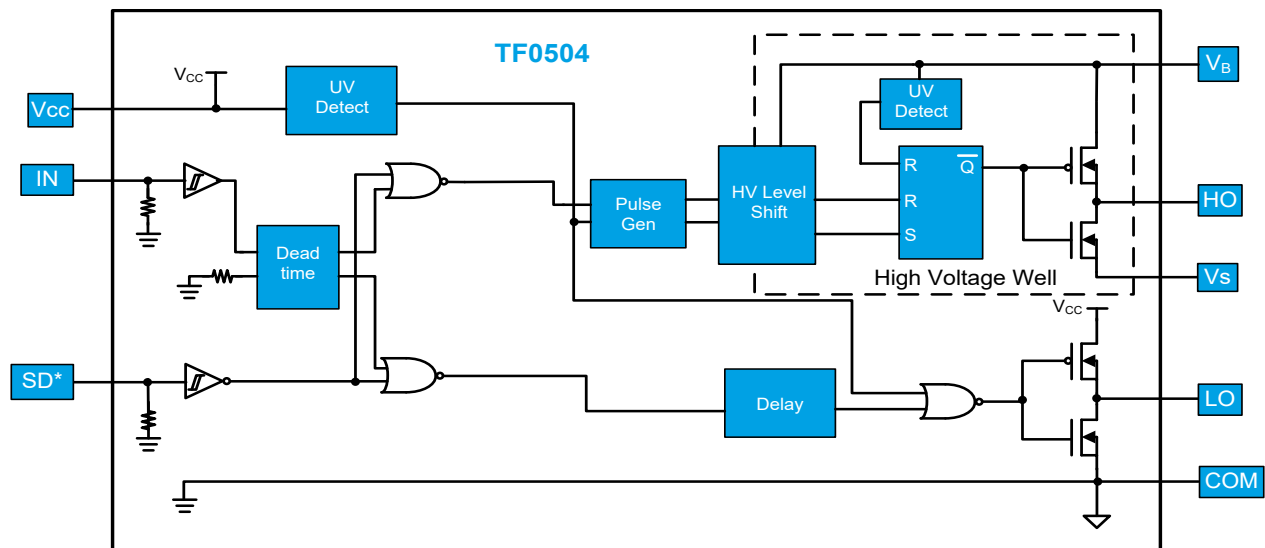
Top View: TDFN-10

TF0504

Pin Descriptions

PIN NAME	PIN NUMBER	PIN DESCRIPTION
V _{CC}	1	Logic and low side supply
IN	2	Logic input for high-side and low-side gate driver outputs (HO and LO), in phase with HO
SD*	3	Logic input for shutdown, enabled low
NC	4, 7	No Connect
COM	5	Low-side and logic return
LO	6	Low-side gate drive output
V _S	8	High-side floating supply return
HO	9	High-side gate drive output
V _B	10	High-side floating supply

Functional Block Diagram





Half-Bridge Gate Driver

Absolute Maximum Ratings (NOTE1)

V_B - High side floating supply voltage.....-0.3V to +124V
 V_S - High side floating supply offset voltage... V_B -24V to V_B +0.3V
 V_{HO} - High side floating output voltage..... V_S -0.3V to V_B +0.3V
 dV_S/dt - Offset supply voltage transient.....50V/ns

V_{CC} - Low-side fixed supply voltage.....-0.3V to +24V
 V_{LO} - Low-side output voltage.....-0.3V to V_{CC} +0.3V
 V_{IN} - Logic input voltage (IN and SD*).....-0.3V to V_{CC} +0.3V

NOTE1 Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

P_D - Package power dissipation at $T_A \leq 25^\circ\text{C}$
 TDFN-10.....0.4W

TDFN-10 Thermal Resistance (NOTE2)

θ_{JA}64°C/W
 θ_{JC}42°C/W

T_J - Junction operating temperature.....+150 °C
 T_L - Lead Temperature (soldering, 10 seconds).....+300 °C
 T_{stg} - Storage temperature-55 to 150 °C

NOTE2 When mounted on a standard JEDEC 2-layer FR-4 board.

Recommended Operating Conditions

Symbol	Parameter	MIN	MAX	Unit
V_B	High side floating supply absolute voltage	$V_S + 10$	$V_S + 20$	V
V_S	High side floating supply offset voltage	NOTE3	100	V
V_{HO}	High side floating output voltage	V_S	V_B	V
V_{CC}	Low side fixed supply voltage	10	20	V
V_{LO}	Low side output voltage	0	V_{CC}	V
V_{IN}	Logic input voltage (IN and SD*)	0	5	V
T_A	Ambient temperature	-40	125	°C

NOTE3 Logic operational for V_S of -5V to +100V. Logic state held for V_S of -5V to $-V_{BS}$



DC Electrical Characteristics (NOTE4)

$V_{BIAS} (V_{CC}, V_{BS}) = 15V, T_A = 25^\circ C$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
V_{IH}	Logic "1" (IN) & Logic "0" (SD*) input voltage	$V_{CC} = 10V$ to $20V$	2.5			V
V_{IL}	Logic "0" (IN) & Logic "1" (SD*) input voltage				0.8	
V_{OH}	High level output voltage, $V_{BIAS} - V_O$	$I_O = 2mA$		0.05	0.2	
V_{OL}	Low level output voltage, V_O	$I_O = 2mA$		0.02	0.1	
I_{LK}	Offset supply leakage current	$V_B = V_S = 100V$			50	μA
I_{BSQ}	Quiescent V_{BS} supply current	$V_{IN} = 0V$ or $5V$		60	100	
I_{CCQ}	Quiescent V_{CC} supply current	$V_{IN} = 0V$ or $5V$		350	500	
I_{IN+}	Logic "1" input bias current	$V_{IN} = 5V, SD^* = 0V$		3	10	
I_{IN-}	Logic "0" input bias current	$V_{IN} = 0V, SD^* = 5V$			5	
V_{CCUV+}	V_{CC} supply under-voltage positive going threshold		7.4	8.5	9.6	V
V_{CCUV-}	V_{CC} supply under-voltage negative going threshold		7.1	7.8	8.8	
V_{BSUV+}	V_{BS} supply under-voltage positive going threshold		5.5	6.5	7.5	V
V_{BSUV-}	V_{BS} supply under-voltage negative going threshold		5.3	6.3	7.3	V
I_{O+}	Output high short circuit pulsed current	$V_O = 0V, PW \leq 10 \mu s$	130	290		mA
I_{O-}	Output low short circuit pulsed current	$V_O = 15V, PW \leq 10 \mu s$	270	600		

NOTE4 The V_{IN} and I_{IN} parameters are applicable to the two logic input pins: IN and SD*. The V_O and I_O parameters are applicable to the respective output pins: HO and LO

**AC Electrical Characteristics**

$V_{BIAS} (V_{CC}, V_{BS}) = 15V$, $C_L = 1000pF$, and $T_A = 25\text{ }^\circ\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	MIN	TYP	MAX	Unit
t_{on}	Turn-on propagation delay	$V_S = 0V$		680	820	ns
t_{off}	Turn-off propagation delay	$V_S = 100V$		150	220	
t_{SD}	Shutdown propagation delay			160	220	
t_{DM}	Delay matching, HS & LS turn-on/turn-off				60	
t_r	Turn-on rise time	$V_S = 0V$		70	170	
t_f	Turn-off fall time			35	90	
t_{DT}	Deadtime: $t_{DT, LO-HO}$ & $t_{DT, HO-LO}$		300	430	550	

Timing Waveforms

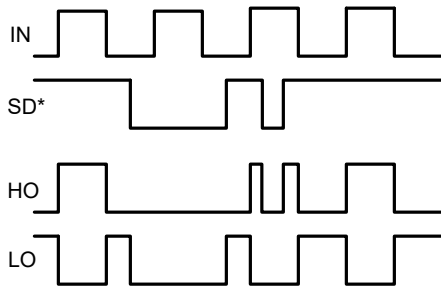


Figure 1. Input / Output Timing Diagram

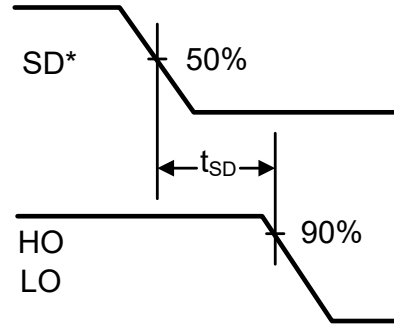
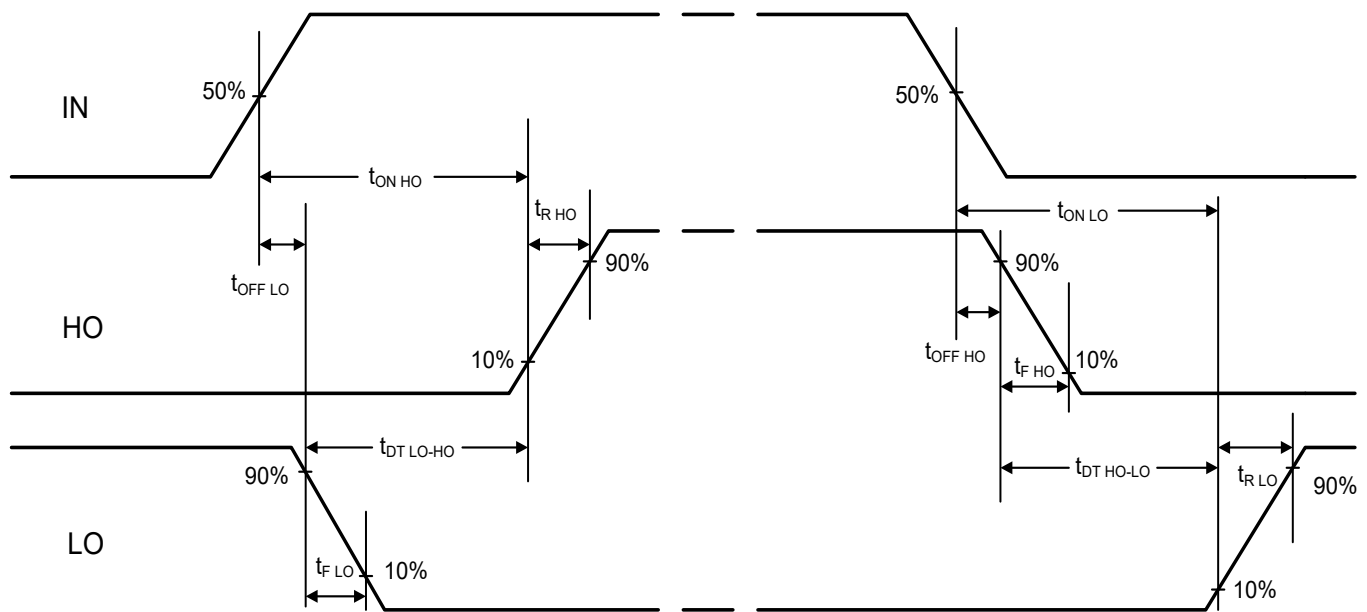


Figure 2. Shutdown Waveform Definition



Deadtime $t_{DT\ LO-HO} = t_{ON\ HO} - t_{OFF\ LO}$
 $t_{DT\ HO-LO} = t_{ON\ LO} - t_{OFF\ HO}$

Deadtime matching
 $t_{MDT} = t_{DT\ LO-HO} - t_{DT\ HO-LO}$

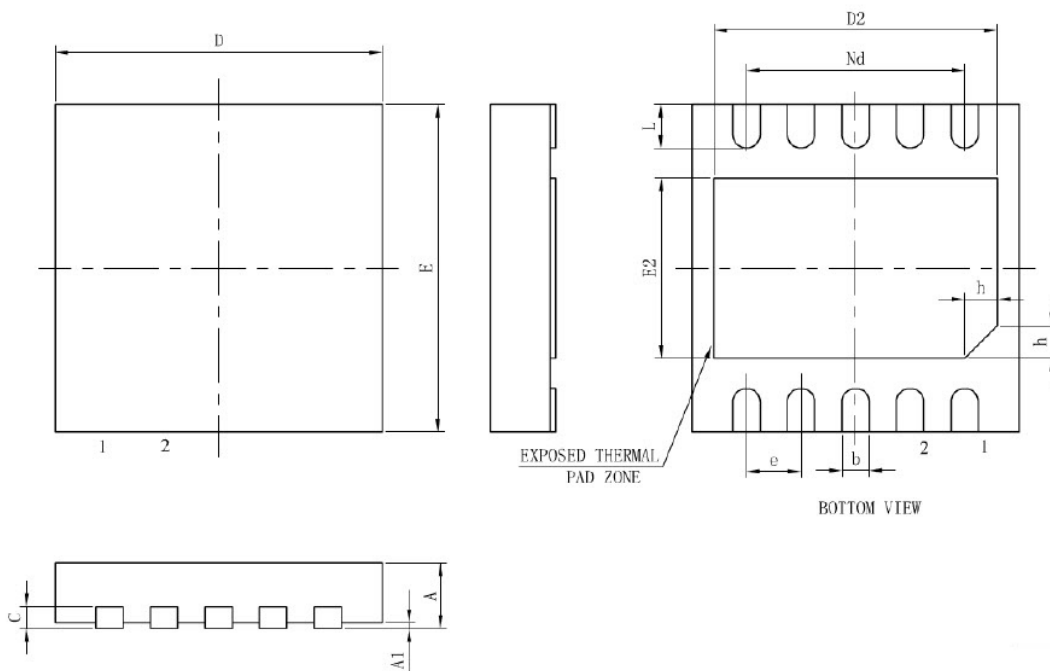
Delay matching
 $t_{DM\ OFF} = t_{OFF\ LO} - t_{OFF\ HO}$
 $t_{DM\ ON} = t_{ON\ LO} - t_{ON\ HO}$

Figure 3. Switching Time Waveform Definitions



Package Dimensions (TDFN-10)

Please contact support@tfsemi.com for package availability.



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	2.40	2.50	2.60
c	0.50BSC		
Nd	2.00BSC		
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
L	0.30	0.40	0.50
h	0.20	0.25	0.30



Revision

Rev.	Change	Owner	Date
2.0	First release, final datasheet	Keith Spaulding	2/6/2016
2.1	Added VBS UVLO block in Functional Block Diagram and to Electrical Specifications	Keith Spaulding	6/28/2016
2.2	Text edit	Keith Spaulding	1/25/2016

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